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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 04509.P010 Total Pages 5

First Named Inventor or Application Identifier Pauline Yeung

Express Mail Label No. EL431887034US

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 16)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 6)

4. X Oath or Declaration (Total Pages 5)

a. X Newly Executed (Original or Copy)

b. ___ Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**

i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ___ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ___ Microfiche Computer Program (Appendix)

7. _____ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. __X__ Assignment Papers (cover sheet & documents(s))
9. _____ a. 37 CFR 3.73(b) Statement (where there is an assignee)
_____ b. Power of Attorney
10. _____ English Translation Document (if applicable)
11. _____ a. Information Disclosure Statement (IDS)/PTO-1449
_____ b. Copies of IDS Citations
12. _____ Preliminary Amendment
13. __X__ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. _____ a. Small Entity Statement(s)
b. Statement filed in prior application, Status still proper and desired
15. _____ Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. __X__ Other: COPY OF POSTCARD WITH EXPRESS MAIL LABEL

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:
___ Continuation ____ Divisional ____ Continuation-in-part (CIP)
of prior application No: _____

18. **Correspondence Address**
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or
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Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: April 7, 2000

Paramita Ghosh

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Serial/Patent No.: unassigned Filing/Issue Date: herewith
Client: Omneon Video Networks
Title: Isochronous Queue And Buffer Management

BSTZ File No.: 04509.P010 Atty/Secty Initials: TMC/PXG/cz
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- ☐ Amendment/Response (____ pgs.)
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- ☐ Application - Rule 1.53(b) Continuation (____ pgs.)
- ☐ Application - Rule 1.53(b) Divisional (____ pgs.)
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- ☐ Application - Rule 1.53(d) CPA Transmittal (____ pgs.)
- ☐ Application - Design (____ pgs.)
- ☐ Application - PCT (____ pgs.)
- ☐ Application - Provisional (____ pgs.)
- ■ Assignment and Cover Sheet
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- ■ Declaration & POA (____ pgs.)
- ☐ Disclosure Docs & Orig & Copy of Inventor's Signed Letter (____ pgs)
- ■ Drawings: 6 # of sheets includes 6 figures
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- ☐ Information Disclosure Statement & PTO-1449 (__ pgs.)
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- ☐ Petition for Extension of Time
- ☐ Petition for ____
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- ☐ Power of Attorney (____ pgs.)
- ☐ Preliminary Amendment (____ pgs.)
- ☐ Reply Brief (____ pgs.)
- ☐ Response to Notice of Missing Parts
- ☐ Small Entity Declaration for Indep. Inventor/Small Business
- ■ Transmittal Letter, in duplicate
- ■ Fee Transmittal, in duplicate
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004509.P010 *Patent*

UNITED STATES PATENT APPLICATION

FOR

ISOCHRONOUS QUEUE AND BUFFER MANAGEMENT

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ISOCHRONOUS QUEUE AND BUFFER MANAGEMENT

FIELD OF THE INVENTION

The present invention relates generally to switches. More specifically, the present invention relates to isochronous queue and buffer management in switches.

BACKGROUND OF THE INVENTION

The IEEE Standard for a High Performance Serial Bus, IEEE Std. 1394-1995 published August 30, 1996 (1394-1995 Standard) and its progeny provide a high speed serial protocol which permits implementation of high speed data transfers. The existing progeny includes P1394a Draft Standard for a High Performance Serial Bus (1394a Standard) and P1394b Draft Standard for a High Performance Serial Bus (1394b Standard). Generically, systems implementing 1394-1995, 1394a, 1394b or subsequent revisions and modifications thereof are referred to herein as 1394 systems.

The IEEE 1394 standard is an international standard for implementing a high-speed serial bus architecture, which supports both asynchronous and isochronous format data transfers. The IEEE 1394 standard defines a bus as a non-cyclic interconnect. Within a non-cyclic interconnect, devices may not be connected together so as to create loops.

In networks, switches filter and forward packets between local area network segments. In packet switching, packets are individually routed between nodes with no previously established communication path. An algorithm is used to route packets to their destination through the most expedient route. The destination computer reassembles the packets in their appropriate order. Packet switching optimizes the use of bandwidth

available in a network and minimizes the latency (the time it takes for a packet to cross a network connection, from sender to receiver).

In a 1394 network with multiple 1394 buses and 1394 switches, all the 1394 buses should be synchronous. But due to cycle skewing, the cycle start packets are not all generated at the same time in different 1394 buses. Cycle skewing occurs when a large asynchronous packet is sent over a bus and the large packet is late, which may delay the start of the next cycle.

In a switch, there may be packets arriving from different ingress ports routed to one egress port. Because of cycle skewing, a packet from one cycle may arrive in the egress port after a packet from a subsequent cycle.

Packets being switched may also be transmitted out of order from the switch because a first packet arriving before a second packet at a switch may not be completely received before the second packet is completely received. Thus, the second packet would be sent out before the first packet because the second packet was completely received before the first packet.

SUMMARY OF THE INVENTION

A method of processing packets in a switch is described. A first queue is selected from at least three queues based on the cycle number (C) of a cycle and flushed at the start of cycle C. At least one isochronous packet is received over a bus during the cycle. The packet is placed in a second queue based on the cycle number.

BRIEF DESCRIPTION OF THE DRAWINGS

Features and advantages of the prevention invention will be apparent to one skilled in the art in light of the following detailed description in which:

Figure 1 is a block diagram of one embodiment of a switch in a communications network;

Figure 2 is a block diagram of one embodiment of a switch;

Figure 3 is a block diagram of packet processing in one embodiment of a switch;

Figure 4 is a block diagram of buffer management in one embodiment of a switch;

Figure 5 is a block diagram of delay adjustment in one embodiment of a switch; and

Figure 6 is a flow diagram for packet processing in one embodiment of a switch.

DETAILED DESCRIPTION

A method and system for a method and system for isochronous queue and buffer management are described.

In the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that the present invention may be practiced without these specific details. In some instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring the present invention.

Figure 1 is a block diagram of one embodiment of the switch in a communications network. Switch 20 is connected to devices 1-5, a wide area network 7 and a local area network 6. Devices 1-5 may include audio, video and/or audio/video devices including storage systems and telecommunications. The wide area network may include the internet or proprietary network or a television communications network.

Figure 2 is a block diagram of one embodiment of a switch. **Figure 2** shows a switch 220 including a processor 228 and a buffer 229. The processor 228 directs operations within the switch 220 and the buffer 229 stores switched packet streams to be transmitted, as described below. Switch 220, according to one embodiment, is configured to switch packets on a IEEE 1394 Standard Serial Bus.

Figure 3 is a block diagram of packet processing in one embodiment of a switch. Figure 3 illustrates a switch 320 having ingress ports 321-324 and egress ports 331-334. The number of ingress ports and egress ports in the switch may vary depending on the application and how many devices or buses are served by the switch.

Each ingress port 321-324 receives a stream of packets. Ingress port 321 receives a stream of packets including packets 311a-b, 312a-b, and 313a-b. Ingress port 322 receives a stream of packets including packets 311c-d, 312c-d, and 313c-d. Ingress port 323 receives a stream of packets including packets 311e-f, 312e-f, and 313e-f. Ingress port 324 receives a stream of packets including packets 311g-h, 312g-h, and 313g-h. Each ingress port 321-324 may be associated with an IEEE Standard 1394 Bus (not shown) or other connections or channels including ethernet, asynchronous transfer mode (atm), T-1 or T-3 carrier, OC-X or any other suitable connection. Packets in packet streams 311-313 may be isochronous packets, according to one embodiment, or any other type of packet that is suitable.

Figure 3 shows packet streams 311-313 arriving at ingress ports 321-324 as follows: packets 311a-h arrive at ingress ports 321-324 during cycle (N) 351, packets 312a-h arrive at ingress ports 321-324 during cycle (N + 1) 352, and packets 312a-h arrive at ingress ports 321-324 during cycle (N + 2) 353.

Figure 3 shows packet stream 311 leaving switch 320 through egress ports 331-334 at cycle (N + 2) 353. Packets 311 arriving at switch 320 at cycle N may be switched during cycles (N), (N + 1) and, possibly (N + 2). The packets 311 are sent out during cycle (N + 2), two cycles after they arrive. As shown in egress cycles 351 and 352, packets 309, which arrived during cycle (N - 2) (not shown) are sent out at cycle (N) 351 and packets 310, which arrived during cycle (N - 1) (not shown) are sent out at cycle (N + 1) 352.

The minimum delay of a 1394 isochronous packet in a 1394 switch is two 1394 cycles. Thus, the 1394 switch 320 uses a buffer management system, as discussed below, to assure that packets arriving at a cycle (N) 351 are sent out in a cycle (N + 2) 353.

Figure 4 is a block diagram of a buffer management system in one embodiment of a switch. In the embodiment shown, buffer management system 450 includes four queues Q0-Q3 451-454 each having a Used pointer 451-454a and a Free pointer 451-454b. Although the buffer management system 450 shown in **figure 4** includes four queues, three queues may be used instead. Each egress port 331-334 has a buffer management system 450 including four queues Q0-Q3 451-454.

In the embodiment shown, packet streams 411, 412, and 413 have arrived at a switch 320. Packet streams 411-413 include packets 411a-411d, 412a-412d and 413a-413d, respectively. The queue numbers correspond to the cycle of the switch 320 in which the packet streams 411-413 will be sent out. As shown by block 435, a packet stream P0(C0) 413, where (C0) represents a time stamp of cycle C0, arrives at cycle C0 and will be sent out at cycle C2.

As egress packet queues 451-454 are filled up, the free pointer values 451-454b are set at free = n, where n represents the point at which packets may be added to queues 451-454. Thus, as shown with reference to Q2 453, free pointer 453b points to the free space after packet 413c, where packet 413d is to be received.

Also, as the packet queues 451-454 are filled up, the used pointer value is set to represent the next packet to be transmitted, as shown by pointers 451-454a. As shown with reference to Q2 453, used pointer 453a is set to 0 and points to space from which the next packet is to be transmitted from the queue Q2 453, through an egress port 331-334

of switch 320. With reference to Q0 451, which is in the process of transmitting packets, the used pointer value 451a equals m, where m represents the space from which the next packet will be sent.

When an packet queue 451-454 is flushed or cleared, a used pointer value 451-454b is set to 0 to show that the space from which the next packet is to be transmitted. As shown with reference to Q3 454 , used pointer 454b points to the space from which the next packet is to be transmitted from queue Q3 454, through an egress port 331-334 of switch 320. Also, when an packet queue 451-454 is flushed or cleared, a free pointer value is set to 0 to show that the queue is empty. As shown with reference to Q3 454 , to show that the queue 454 is free, 454a is set to 0 to point to the place in queue Q3 454 where the next packet may be placed.

At any given cycle C of the switch 320, there are isochronous packets in the switch 320 which arrived in cycle C, C - 1 557, and C - 2 556. To guarantee the packets are sent in the proper cycle, at least three packet queues are needed for every egress port.

Figure 5 is a block diagram of delay adjustment in one embodiment of a switch. A delay adjustment may become necessary where cycle skewing, as described above, occurs. A switch 320 includes an inbound cycle 525, a transition cycle 526 and an outbound cycle 527. Packet streams 511a-d, 512a-d, 513a-d, and 514a-d are received at switch 320 during cycles C - 3 555, C - 2 556, C - 1 557, and C 558 of the inbound cycle of the switch.

In the embodiment shown, input packets 511 comes in at inbound cycle C - 3 555 and input packets 512 starts to come in at inbound cycle C - 2 556 of inbound cycle 525. However input packet stream 512 includes packet 512d which comes in at the end of

cycle C - 2 556 and almost in cycle C - 1 557. Thus, cycle C - 2 556 is expanded from 556a to accommodate the late packet and cycle C - 1 557 is shortened.

In transition cycle 526, packets 512a and 512b of input packets 512 are switched during cycle C - 2 556 and placed in the appropriate egress packet queue 451-454, while packets 512c and 512d are switched at cycle C - 1 557 and placed in the appropriate packet queue 451-454. Because packets 512 arrived during inbound cycle C - 2 556, it will be buffered to go out at cycle C even though a few of the packets were late. Thus, input packets 512 is sent out at cycle C 558 of outbound cycle 527.

Packets 511, received at cycle C - 3 555 is switched during cycle C - 2 556 of the transition cycle, and sent out at cycle C - 1 557. However, packets 511 need not be switched at cycle C - 2 556. Packets 513, which is received during cycle C - 1 557 is switched during cycles C -1 557 and C 558, and will be sent out during cycle C + 1, not shown. Packet 513a is switched during cycle C - 1 557 and packets 513b-d are switched during cycle C 558. Also, as shown, packets 514a-b are switched at cycle C 558, the cycle during which packets 514 was input.

Figure 6 is a flow diagram for packet processing in one embodiment of a switch. At processing block 671, a first queue is selected based on the cycle number of the egress cycle of the switch 220. At processing block 672, the first queue is flushed at the start of the cycle. At processing block 673, an isochronous packet is received over a bus. At processing block 674, the packet is placed in a packet queue based on the cycle number of the cycle. The multiple packet queues Q0-Q3 451-454 are used in each egress port of the 1394 switch to resolve the order of packets that will depart in different cycles according to the egress 1394 cycle time.

Thus, if n queues are used for each port, where $n \geq 3$, packets that arrived in cycle C would go to queue number (C + 2) % n (where % stands for remainder). In cycle C, the egress port sends packets from queue (C % n). Thus, if cycle number C is 5 and the number of queues equals 4, the egress port will send packets from queue number Q1, since the remainder of (5 / 4) is one.

When a packet stream 411 arrives at the egress port, as represented in processing block 673, a packet buffer 451-454 is allocated from the packet buffer pool to hold the complete packet. When this packet departs, there is no need to free the memory associated with this packet buffer. Rather at the beginning of each cycle C, all memory in the packet buffer pool associated with packet queue number (C - 1) % n is reclaimed. Thus if the cycle number is 5 and the number of queues equals 4, Q0 451 would be flushed at the beginning of cycle five while Q1 is being filled up. Thus, the queue being filled, the queue being flushed and the queue having packets transmitted are all based on the cycle number of the 1394 switch.

In the foregoing specification, the invention has been described with reference to specific embodiments thereof. It will, however, be evident that various modifications and changes can be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

Claims

I claim:

1. A method of processing packets in a switch comprising:

selecting a first queue from at least three queues in a switch based on the cycle number (C) of a cycle;

flushing the first queue at the start of the cycle;

receiving at least one isochronous packet over a bus during the cycle;

placing the packet in a second queue based on the cycle number.

2. The method of claim 1 further comprising:

transmitting the packet from the second queue after two cycles.

3. The method of claim 1 wherein the first queue is chosen from four queues.

4. The method of claim 1 wherein the first queue is associated with a cycle that has a cycle number of C minus 1.

5. The method of claim 1 wherein the first queue is the same as the second queue.

6. The method of claim 1 wherein the first queue number is equal to the remainder of (C-1)/n wherein n is the number of queues in the switch.

7. The method of claim 1 wherein the second queue number is equal to the remainder of (C+2)/n wherein n is the number of queues in the switch.

8. The method of claim 1 further comprising:

transmitting packets in cycle C from a third queue wherein the queue number of the third queue is equal to the remainder of C/n wherein n is the number of queues in the switch.

9. The method of claim 1 further comprising:

setting a free pointer in the first queue to 0 at the end of the cycle; and

setting a used pointer in the first queue to 0.

10. The method of claim 1 further comprising:

setting a used pointer in the second queue to 0 at the end of the cycle; and

setting a free pointer in the second queue to n.

11. A system of processing packets in a bus switch comprising:

means for storing data in queues;

means for selecting appropriate queuing means for each set of incoming data;

means for directing the set of incoming data to the appropriate queuing means; and

means for flushing data from the queuing means.

12. The system of claim 11 further comprising means for receiving the incoming data and wherein the incoming data includes isochronous packets.

13. A switch in a network comprising:

a buffer memory including at least three egress queues; and

a processor configured to direct incoming isochronous packets into one of the egress queues based on a cycle number of the switch and configured flush another of the egress queues based on the cycle number.

14. The switch of claim 13 wherein the switch is configured to be used with at least one bus.

15. The switch of claim 13 wherein the switch is configured to be used with a connection selected from the group: ethernet bus, asynchronous transfer mode bus, and IEEE 1394 standard bus.

16. The switch of claim 13 further comprising:

at least one ingress port; and

at least one egress port

wherein each egress port is associated with at least three egress queues.

17. The switch of claim 16 wherein the egress queues store data to be transmitted by the processor from each egress port.

18. The switch of claim 13 wherein the buffer memory includes four queues.

19. The switch of claim 13 wherein the processor is configured to direct the incoming isochronous packets into the egress queue number equal to the remainder of (C + 2)/n wherein n is the number of queues in the switch.

20. The switch of claim 13 wherein the processor is configured to flush the egress queue number equal to the remainder of (C - 1)/n wherein n is the number of queues in the switch.

21. The switch of claim 13 wherein the processor is configured to transmit the isochronous packets from the egress queue number equal to the remainder of C/n wherein n is the number of queues in the switch.

ABSTRACT

A method of processing packets in a switch. A first queue is selected from at least three queues based on the cycle number (C) of a cycle and flushed at the start of cycle C. At least one isochronous packet is received over a bus during the cycle. The packet is placed in a second queue based on the cycle number.

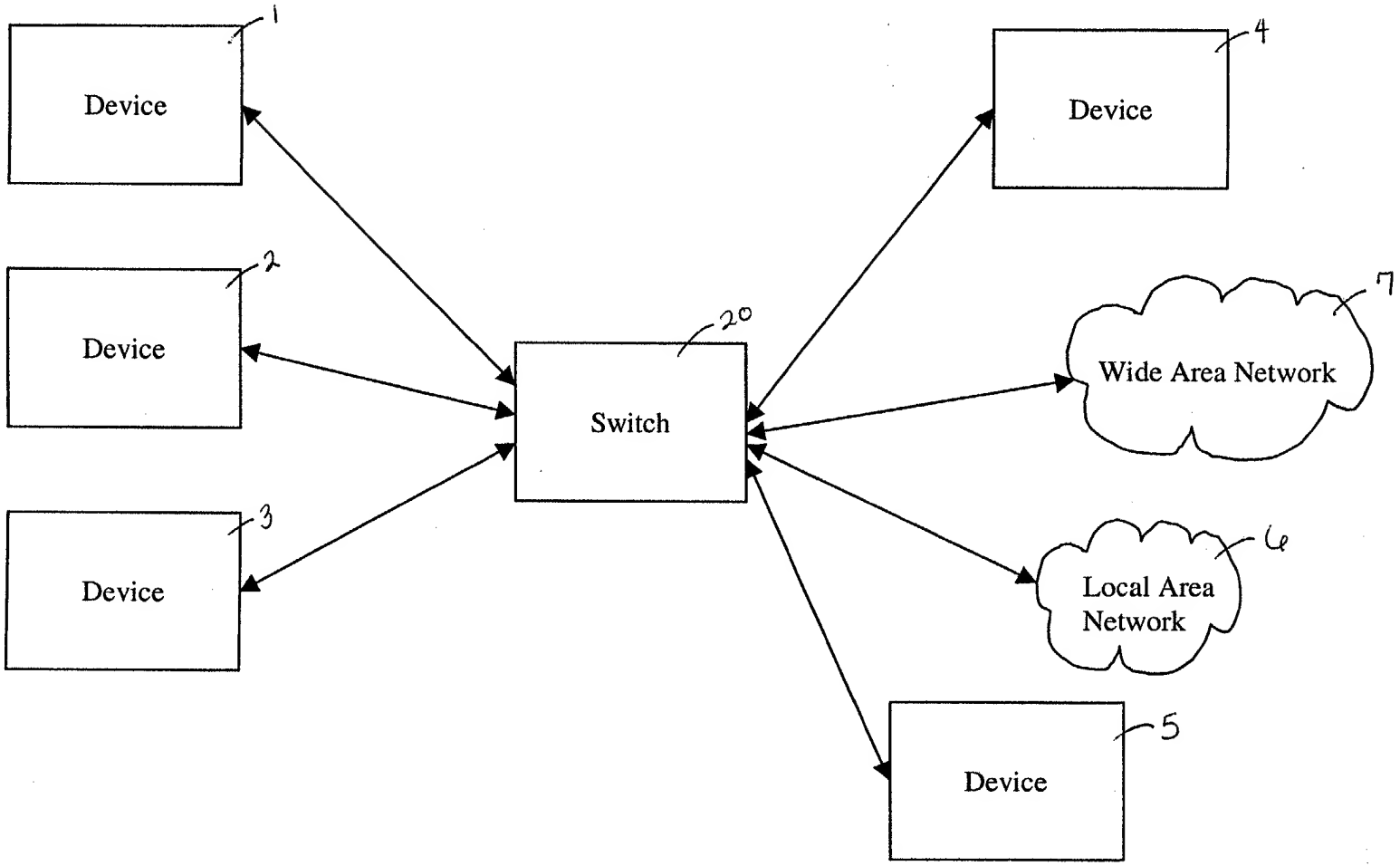


Figure 1

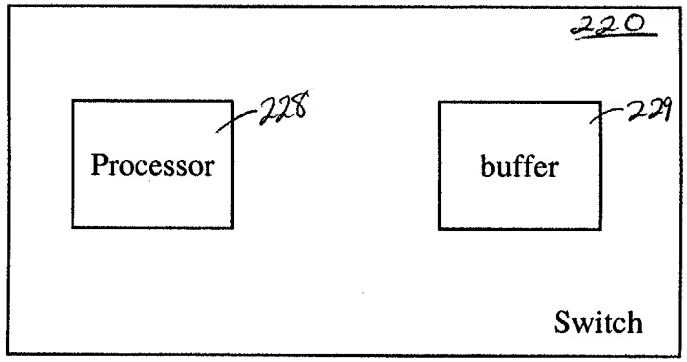
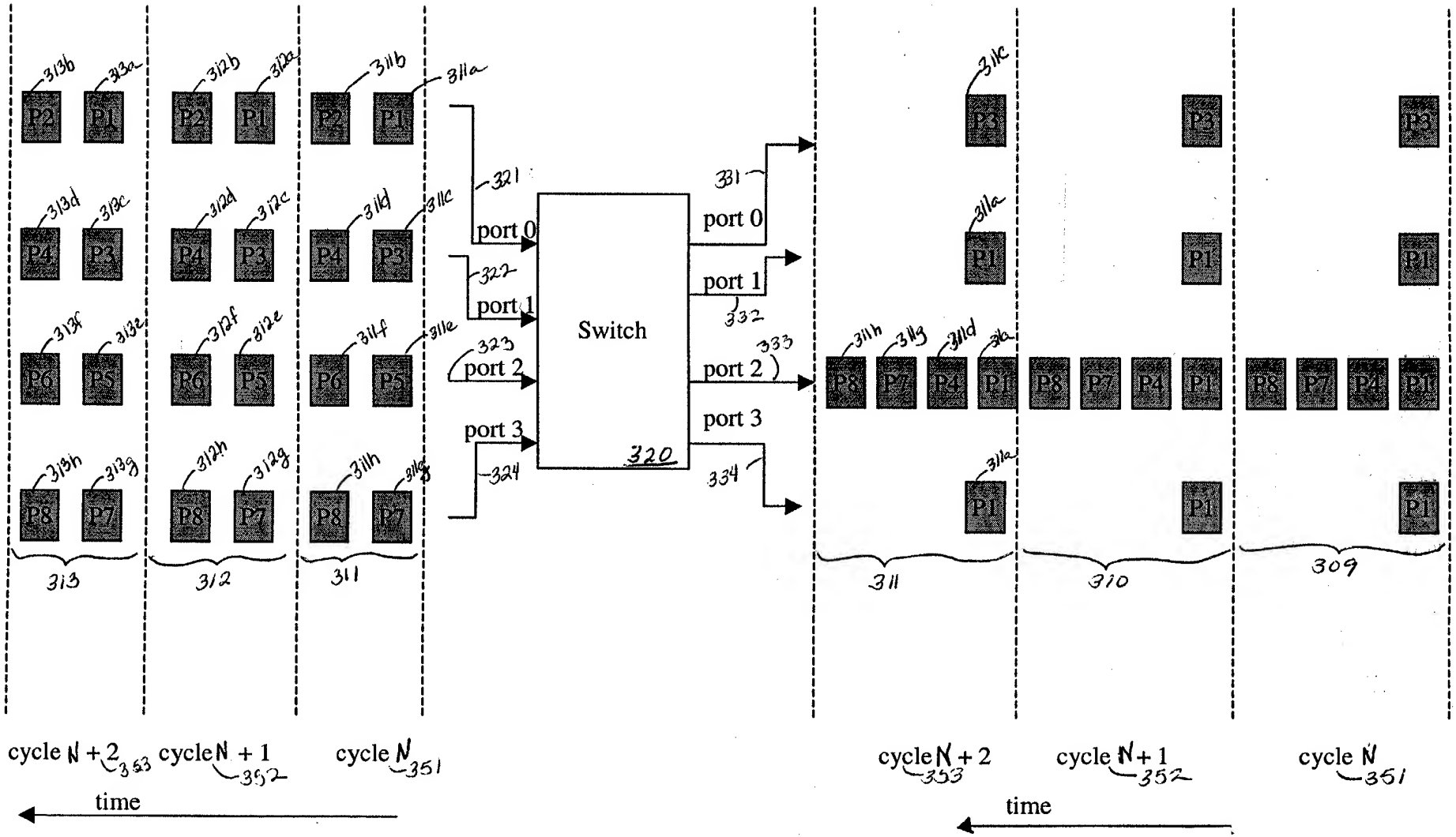


Figure 2


P2
P1
P4
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P8
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313
312
311
310
309
port 0
port 1
port 2
port 3
Switch
320
321
322
323
324
331
332
333
334
cycle N + 2
353
cycle N + 1
352
cycle N
351
time

Figure 3

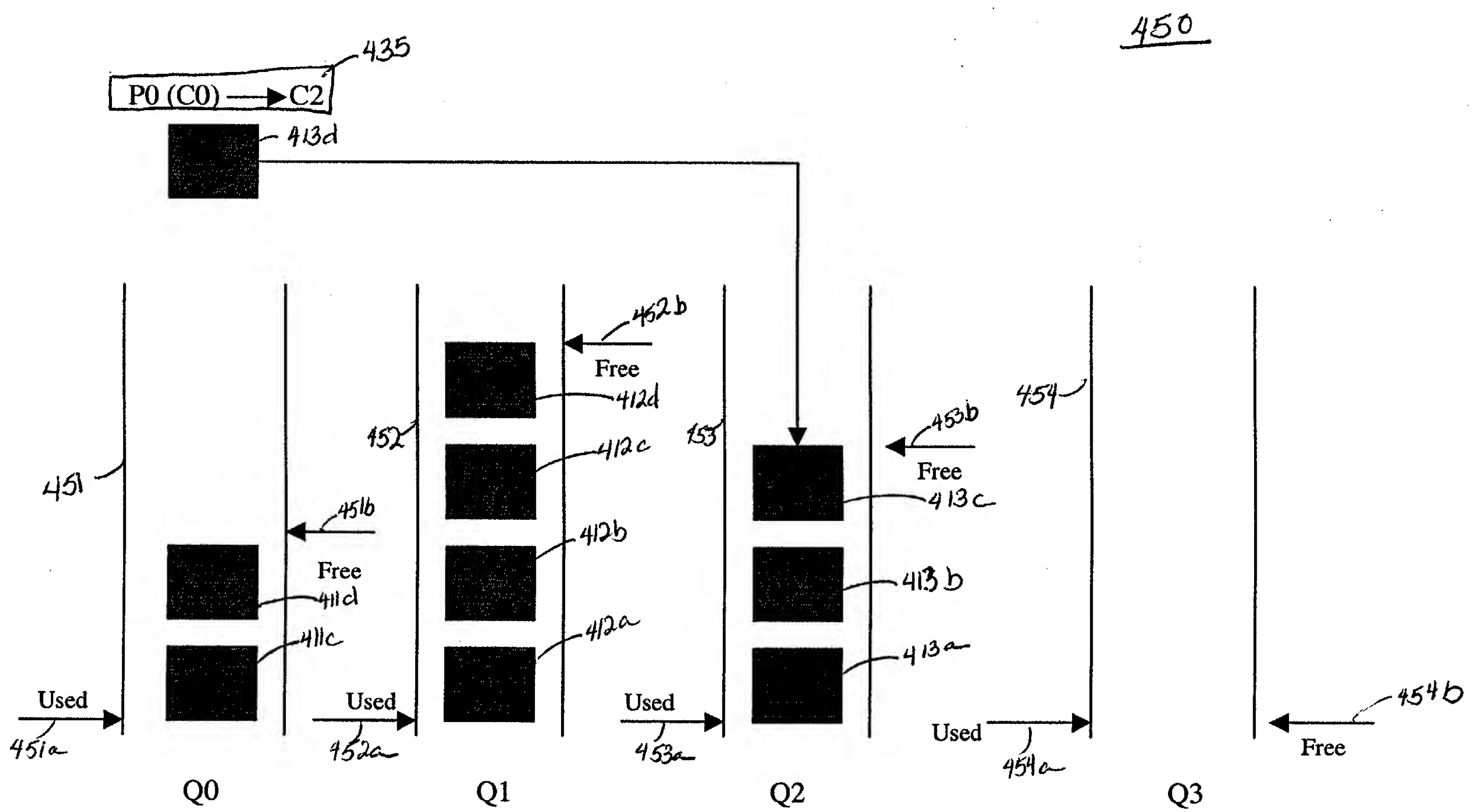
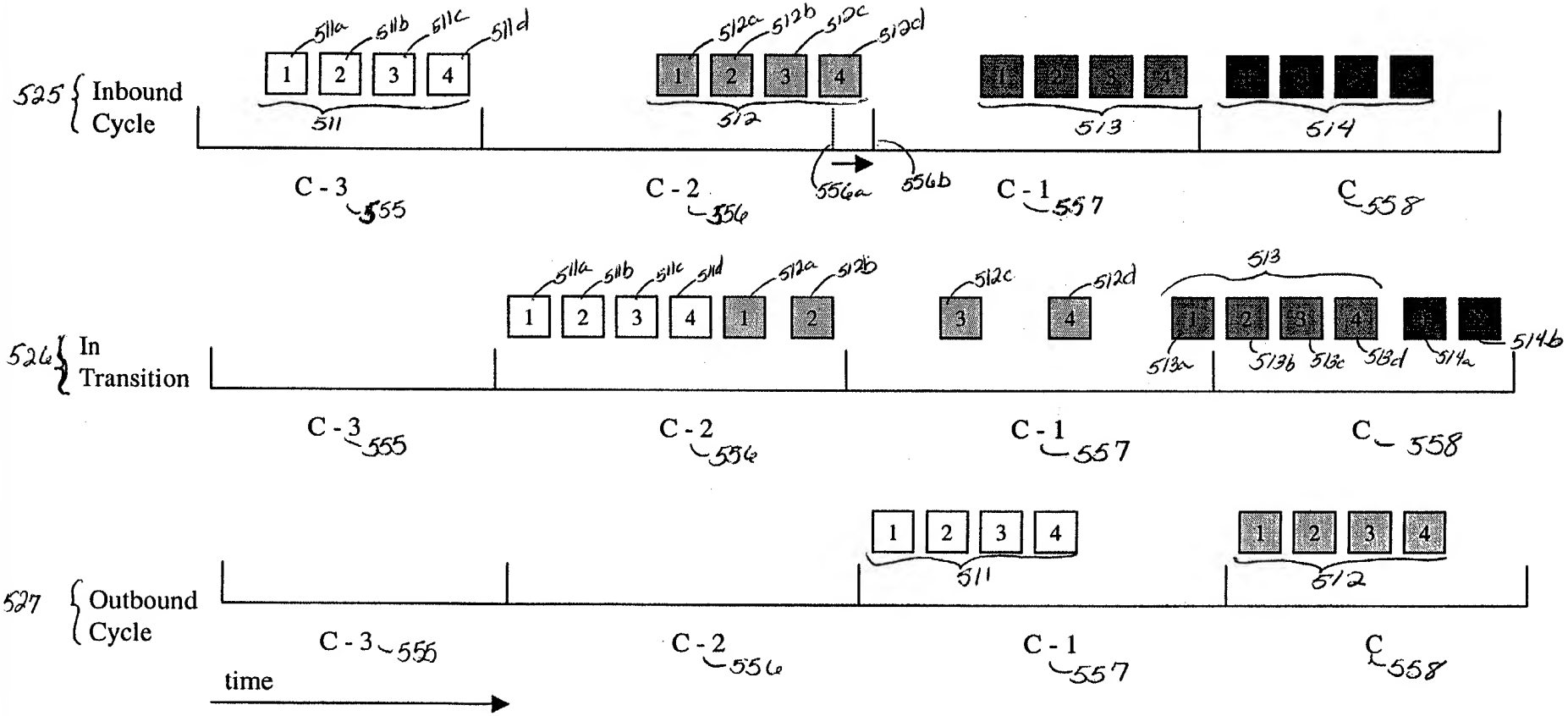


Figure 4


525
Inbound Cycle
511a
511b
511c
511d
1
2
3
4
511
512a
512b
512c
512d
512
513
514
C - 3
555
C - 2
556
556a
556b
C - 1
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In Transition
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513c
513d
514a
514b
527
Outbound Cycle
time

Figure 5

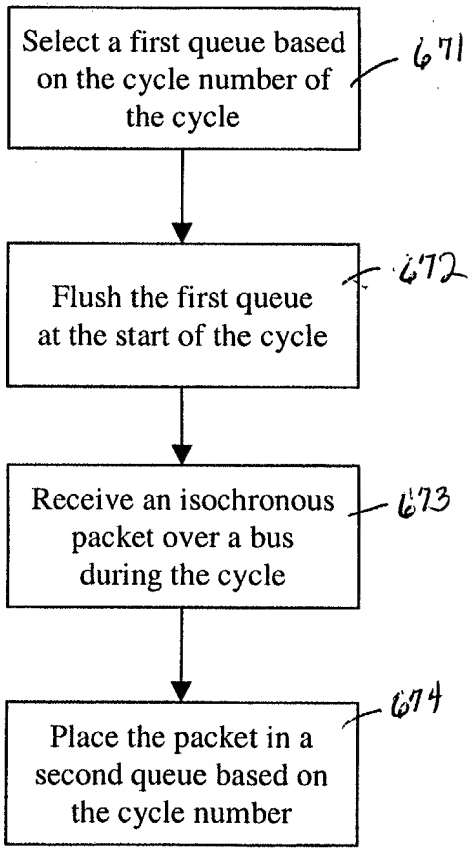
Select a first queue based on the cycle number of the cycle
671
Flush the first queue at the start of the cycle
672
Receive an isochronous packet over a bus during the cycle
673
Place the packet in a second queue based on the cycle number
674

Figure 6

Attorney's Docket No.: 04509.P010 Patent

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

ISOCHRONOUS QUEUE AND BUFFER MANAGEMENT

the specification of which

__x__ is attached hereto.
____ was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

(Application Number)	Filing Date
(Application Number)	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)	Filing Date	(Status -- patented, pending, abandoned)
(Application Number)	Filing Date	(Status -- patented, pending, abandoned)

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Paramita Ghosh, BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to Paramita Ghosh, (408) 720-8300.

(Name of Attorney or Agent)

(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor Pauline Sai-Fun Yeung

Inventor's Signature Pauline SF Yeung Date April 6, 2000

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Full Name of Fourth/Joint Inventor _____

Inventor's Signature _____ Date _____

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APPENDIX A

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APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.